## Claims

1. A method of making integrated circuits, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first conductive structure on the first mask layer, with the first conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second conductive structure on the second mask layer, with one or more portions of the second conductive structure contacting at least one of the exposed portions of the first conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second conductive structures after forming the diffusion barrier.

2. The method of claim 1

wherein forming the first and second mask layers comprises depositing photoresist; and

wherein forming the first and second conductive structures comprises filling one or more of the openings or trenches with a copper-, silver-, or gold-based material.

3. The method of claim 1:

wherein removing the first and second mask layers comprises ashing the first and second mask layers;

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second conductive structures with an aerogel or xerogel.

4. A method of making integrated circuits, comprising:

a step for forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

a step for forming a first conductive structure on the first mask layer, with the first conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

a step for forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

a step for forming a second conductive structure on the second mask layer, with one or more portions of the second conductive structure contacting at least one of the exposed portions of the first conductive structure;

a step for removing concurrently at least respective portions of the first and second mask structures after forming the second conductive structure;

a step for forming a diffusion barrier on at least respective portions of the first and second conductive structures after removing at least the respective portions of the first and second mask structures; and

a step for forming an insulator on and between the first and second conductive structures after forming the diffusion barrier.

5. A method comprising:

forming a conductive structure;

forming a diffusion-barrier lining around the conductive structure after forming the conductive structure; and

forming an insulative structure around the conductive structure after forming the diffusion-barrier lining.

6. The method of claim 5, wherein forming the conductive structures comprises applying a copper-, silver-, or gold-based material.

7. The method of claim 5, wherein forming the conductive structure comprises:

ionized sputtering or DC magnetron sputtering of a copper-based material onto at least a portion of the diffusion barrier; and

electroplating a copper-based material onto the sputtered copper-based material.

8. The method of claim 5, wherein forming the insulative structure comprises spin-coating an aerogel or xerogel.

9. The method of claim 5, wherein forming the diffusion-barrier lining comprises forming a graded composition of $WSi_x$, where x varies from 2.0 to 2.5.

10. The method of claim 5, wherein forming the diffusion-barrier lining comprises:

forming a graded composition of $WSi_x$, where x varies from 2.0 to 2.5; and

nitriding the graded composition of $WSi_x$.

11. The method of claim 5 wherein nitriding the graded composition of $WSi_x$ comprises exciting a plasma with argon gas.

12. The method of claim 5, wherein forming the diffusion-barrier lining comprises:

introducing tungsten hexaflouride and hydrogen gases into a wafer processing chamber for a predetermined amount of time;

introducing silane gas into the chamber a first predetermined time after introducing the tungsten hexaflouride gas; and

terminating introduction of the silane gas a second predetermined time before terminating introduction of the tungsten hexaflouride and hydrogen gases into the chamber.

13. The method of claim 5, wherein the first and second times are in the range of about one to about three seconds.

14. A method comprising:

a step for forming a conductive structure;

a step for forming a diffusion-barrier lining around the conductive structure after forming the conductive structure; and

a step for forming an insulative structure around the conductive structure after forming the diffusion-barrier lining.

15. A method comprising:

forming a first mask in an integrated-circuit assembly;

forming a first conductor on the first mask;

forming a second mask on the first conductor;

forming a second conductor on the second mask; and

removing at least respective portions of the first and second masks in a single material-removal procedure.

16. The method of claim 15, wherein removing at least respective portions of the first and second mask in the single material-removal procedure comprises removing substantially all of the first and second masks.

17. The method of claim 15, wherein removing at least respective portions of the first and second masks comprises ashing the first and second masks.

18. The method of claim 15, wherein forming the first mask and forming the second mask each comprise applying a photoresist to a surface in the integrated circuit assembly using spincoating.

19. The method of claim 15, wherein forming the first conductor or forming the second conductor comprises applying a copper-, silver-, or gold-based material to a surface in the integrated-circuit assembly.

20. The method of claim 15, wherein forming the first conductor comprises:

ionized sputtering or DC magnetron sputtering of a copper-based material onto at least a portion of the diffusion barrier; and

electroplating copper-based material onto the sputtered copper-based material.

21. A method comprising:

a step for forming a first mask in an integrated-circuit assembly;

a step for forming a first conductor on the first mask;

a step for forming a second mask on the first conductor;

a step for forming a second conductor on the second mask; and

a step for removing respective portions of at least the first and second mask in a single material-removal procedure.

22. A method comprising:

forming a first wiring level in an integrated circuit assembly;

forming a second wiring level in the integrated circuit assembly, the second wiring level electrically coupled to the first wiring level; and

forming a diffusion barrier around at least a portion of the first wiring level and at least a portion of the second wiring level in a single barrier-formation procedure.

23. The method of claim 22, wherein forming the first wiring level or forming the second wiring level comprises applying a copper-, silver-, or gold-based material to a surface in the integrated-circuit assembly.

24. The method of claim 22, wherein the first wiring layer includes one or more first substantially planar portions and the second wiring layer includes one or more second substantially planar portions which are substantially parallel to the first substantially planar portions.

25. The method of claim 22, wherein forming the first wiring layer comprises:

ionized sputtering or DC magnetron sputtering of a copper-based material onto at least a portion of the diffusion barrier; and

electroplating copper-based material onto the sputtered copper-based material.

26. The method of claim 22, wherein forming the diffusion-barrier lining comprises:

introducing tungsten hexaflouride and hydrogen gases into a wafer processing chamber for a predetermined amount of time;

introducing silane gas into the chamber a first predetermined time after introducing the tungsten hexaflouride gas; and

terminating introduction of the silane gas a second predetermined time before terminating introduction of the tungsten hexaflouride and hydrogen gases into the chamber.

27. A method comprising:

forming a first wiring level in an integrated circuit assembly;

forming a second wiring level in the integrated circuit assembly; and

forming a diffusion barrier around at least a portion of the first wiring level and at least a portion of the second wiring level in a single barrier-formation procedure.

28. The method of claim 27, further comprising:

forming a third wiring level in the integrated-circuit assembly after forming the second wiring level, wherein forming the diffusion barrier in the single barrier-formation procedure forms at least a portion of the includes insulative structure occurs after forming the first, second, and third wiring levels.

29. A method comprising:

a step for forming a first wiring level in an integrated circuit assembly;

a step for forming a second wiring level in the integrated circuit assembly; and

a step for forming a diffusion barrier around at least a portion of the first wiring level and at least a portion of the second wiring level in a single barrier-formation procedure.

30. A method comprising:

forming a first wiring level in an integrated-circuit assembly;

forming a second wiring level in the integrated-circuit assembly; and

forming an insulative structure having at least a portion between the first and second wiring levels after forming the second wiring level.

31. The method of claim 30, further comprising:

forming a third wiring level in the integrated-circuit assembly after forming the second wiring level, wherein forming the insulative structure occurs after forming the first, second, and third wiring levels.

32. A method comprising:

forming a first structure having one or more trenches or openings;

forming a conductive structure in at least one of the trenches or openings;

removing substantially all of the first structure to define a space around the conductive structure;

applying a diffusion-barrier material to at least a portion of the conductive structure after removing substantially all of the first structure;

forming an insulative structure on at least a portion of the diffusion-barrier material applied to the conductive structure.

33. A method comprising:

forming a non-conductive structure having one or more trenches or openings;

forming a conductive structure in at least one of the trenches or openings;

removing substantially all of the non-conductive structure to define a space around the conductive structure;

applying a diffusion-barrier material to at least a portion of the conductive structure after removing substantially all of the non-conductive structure;

forming an insulative structure on at least a portion of the diffusion-barrier material applied to the conductive structure.

34. The method of claim 33, wherein the diffusion-barrier material contacts a surface of the conductive structure.

35. A method of making integrated circuits, comprising:

providing a layer including one or more transistors, with each transistor having one or more transistor contact regions;

forming a first mask layer having one or more openings, with each opening exposing at least a portion of at least one of the transistor contact regions;

forming a first conductive structure over the first mask layer and contacting one or more of the transistor contact regions;

forming a second mask layer having one or more openings, with each opening exposing at least a portion of the first conductive structure;

forming a second conductive structure over the second mask layer, with the second conductive structure contacting one or more exposed portions of the first conductive structure;

removing substantially all of the first and second mask structures after forming the second conductive structure;

forming a diffusion barrier on least the first and second conductive structures after removing substantially all of the first and second mask structures;

forming an insulative material between at least a portion of the first conductive structure and at least a portion of the second conductive structure after removing substantially all of the first and second mask structures.

36. A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first gold-based conductive structure on the first mask layer, with the first gold-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second gold-based conductive structure on the second mask layer, with one or more portions of the second gold-based conductive structure contacting at least one of the exposed portions of the first gold-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second gold-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second gold-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second gold-based conductive structures after forming the diffusion barrier.

37. The method of claim 36:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second gold-based conductive structures with an aerogel or xerogel.

38. A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first silver-based conductive structure on the first mask layer, with the first silver-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second silver-based conductive structure on the second mask layer, with one or more portions of the second silver-based conductive structure contacting at least one of the exposed portions of the first silver-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second silver-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second silver-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second silver-based conductive structures after forming the diffusion barrier.

39. The method of claim 38:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second silver-based conductive structures with an aerogel or xerogel.

40. A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first copper-based conductive structure on the first mask layer, with the first copper-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second copper-based conductive structure on the second mask layer, with one or more portions of the second copper-based conductive structure contacting at least one of the exposed portions of the first copper-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second copper-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second copper-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second copper-based conductive structures after forming the diffusion barrier.

41. The method of claim 40:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second copper-based conductive structures with an aerogel or xerogel.

42. An integrated-memory-circuit assembly comprising:

a surface having one or more transistor regions;

a first copper-, silver-, or gold-based wiring level having one or more first portions coupled to one or more of the transistors, the one or more first portions having a first diffusion-barrier lining and defining a substantially horizontal first plane, with the first plane and the surface defining a first open region; and

at least a second copper-, silver-, or gold-based wiring level having one or more second portions electrically coupled and attached to the first gold-based wiring level, the one or more second portions having a second diffusion-barrier lining and defining a substantially horizontal second plane which is substantially parallel to the first plane, with the first and second planes defining a second open region.